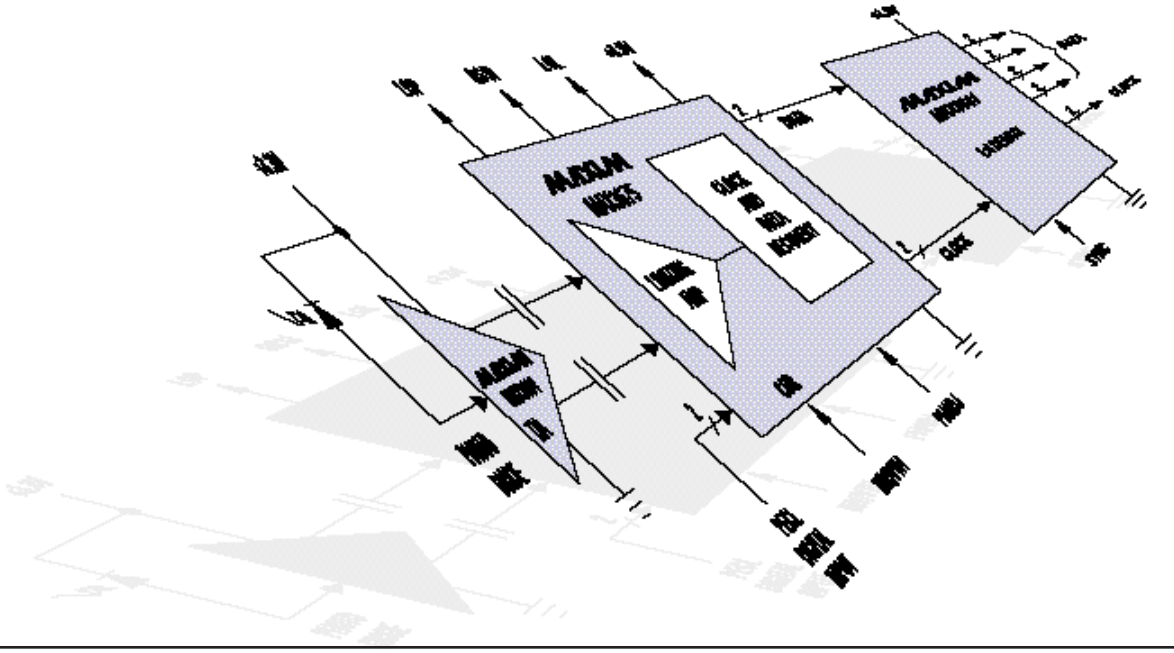
MAXIM Engineering Journal

Special Fiber Optic Edition



News Briefs

MAXIM REPORTS RESULTS FOR THE FIRST QUARTER OF FISCAL 1999

Maxim Integrated Products, Inc., (MXIM) reported net revenues of $155.3 million for the first quarter of fiscal 1999 ending September 26, 1998, compared to $125 million for the same quarter in fiscal 1998. Net income increased to a record $49.4 million in Q199, compared to $40 million for the first quarter of fiscal 1998. Income per share increased to $0.33 for Q199, compared to $0.26 for the same period a year ago.

During the quarter, the Company increased cash and short-term investments by $19.1 million after paying $43.5 million for 1.4 million shares of its common stock and $12.5 million for capital equipment. Inventory remained flat with Q498, and accounts receivable declined by $2.4 million during the quarter. Annualized return on average stockholders' equity during the quarter was 31%, one of the highest in the industry today.

During Q199, shipments to customers remained at Q498 levels despite global economic conditions and lower end market bookings than in the previous quarter. Turns orders received during the quarter increased 21% over the Q498 level and were approximately $42 million (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders).

In addition to the increased level of turns orders received during the quarter, the Company also experienced a higher percentage of orders requesting near-term delivery (customer orders for delivery in Q199 or Q299).

We attribute the prevalence of short-term orders to our reduced lead times, and limited customer expectations for short-term improvement in demand for end-market equipment. We also believe that the economic uncertainty in the world markets is negatively affecting the inventory and purchasing psychology of the Company's customers, resulting in less long-term ordering. Net bookings during the quarter were approximately $127 million, a 7% decline from Q498. First quarter ending backlog shippable within the next 12 months was approximately $143.2 million, a decline from the $181 million reported at the end of Q498. Eighty percent of the ending Q199 backlog consists of orders that were requested for shipment in Q299 or earlier.

Gross margins for the first quarter were consistent with Q498 at 67.5%. During Q199, the Company recorded charges of $2.3 million related to obsoleting of a 4-inch wafer fabrication facility. This capacity was replaced by a 6-inch sub-micron facility acquired in November 1997, which is now in production. The Company also expensed approximately $2.8 million of manufacturing costs that were in excess of the costs achieved by the Company's lowest cost wafer fabrication facility (Beaverton). In addition, the Company increased its reserves for inventory by $2.2 million, further increasing cost of sales in Q199.

Jack Gifford, Chairman, President and Chief Executive Officer, commented: "Current worldwide economic uncertainties are impacting our customers' ability to predict the demand for their products. In this environment, prudence dictates that we remain cautious about our short-term revenue outlook. To maintain our current revenue level, we will need a continued increase in turns orders that match available supply and an overall increase in the order rate from the Q199 levels."

Gifford commented further: "In Q199, none of the geographic or end equipment markets broke out of the downward booking trend of the last three quarters. We continue to watch for a leading indicator predicting a change in the ordering rates from the last nine months. We believe that customer inventories are not large and any change in our customers' perception regarding the direction of the world economy could cause a significant increase in demand."

Mr. Gifford continued: "Maxim's competitive position has never been better. The Company's product line continues to be the broadest in the industry, and its customer base is very large and spreads across all major geographic regions in the world. Our rate of new product announcements continues to be unrivaled in our industry. In the past, our new product proliferation has strongly correlated to our growth rate. We believe this trend will continue."

Optical/electrical conversion in SDH/SONET fiber optic systems

The advent of cheaper and more powerful personal computers has not only expanded the user base; it is also creating a demand for greater transmission capacity among the telecom networks by adding an increasing volume of internet and videophone connections to the traditional phone and fax services. The following discussion of an OC 12/STM 4 receiver/transmitter chipset supports these developments and includes a description of the electronic components required for optic/electric (O/E) conversion in SDH/SONET fiber optic transmission systems.

Competition among network providers enables the multimedia market to grow, and the introduction of new and improved products and services in the near future should strengthen the demand for increased transmission capacity. This need for more data throughput can be satisfied economically with fiber optic (FO) cables because the transmission capacity is potentially very high (versus that of copper wires). The physical nature of the fiber cable lets providers expand capacity by increasing the transmission bit rate or by introducing alternative transmission techniques, without the need for further upgrades or additional cable installations. These advantages have led many countries to build extensive fiber networks, and further expansion of these networks can be expected.

To transmit optical data via fiber cables, signals must be converted from electrical to optical at the transmit end, and then converted back to electrical at the receive end. These necessary conversions are handled by receiver/transmitter units that contain electronic devices along with the optical components.

FO transceivers

The widely used Time Division Multiplex (TDM) transmission technique now enables bit rates up to 10Gbps and is well established in modern transport systems.

Today's high-speed fiber optic transmission systems offer the following standard bit rates:

SONET STANDARD	SDH STANDARD	BIT RATE
OC 1	—	51.84Mbps
OC 3	STM 1	155.52Mbps
OC 12	STM 4	622.08Mbps
OC 48	STM 16	2.4883Gbps
OC 192	STM 64	9.9533Gbps

New techniques such as Wavelength Division Multiplexing (WDM) further increase the transmission capacity by sending numerous time-multiplexed data streams over one fiber, using a different wavelength for each data stream. Electronic components in a WDM receiver and transmitter (compared with those in a TDM system) differ according to the behavior of the optical sources and line amplifiers in the WDM transport system. The following section describes the performance required for receivers and transmitters in an optical TDM transmission system.

Optical receivers

Optical receivers detect optical signals from the fiber and convert them to electrical signals, which must then be amplified before their data waveforms and clock can be recovered. A serial-to-parallel conversion of the data stream may be necessary, depending on the bit rate and the system-specific setup of the following CMOS functions. **Figure 1** shows how the receiver's output interface provides regenerated data in a serial or parallel bit stream, along with the recovered clock.

A PIN or APD (avalanche photodiode) photodetector converts the received light to a signal current. The PIN diode is relatively cheap and operates with the same supply voltage as the electronic components, but for a given optical power it generates fewer electrons than the APD. As a result, the APD provides a more sensitive receiver that can be placed farther away from the transmitter. This advantage is offset by the need for an APD bias circuit, which (depending on the APD type) must provide a reverse operating voltage in the 30V to 100V range. Additionally, the APD adds more noise, costs more, and requires cooling.

The photodetector delivers the extracted current to a transimpedance amplifier (TIA), which first converts the current to a voltage. This single-ended voltage is then

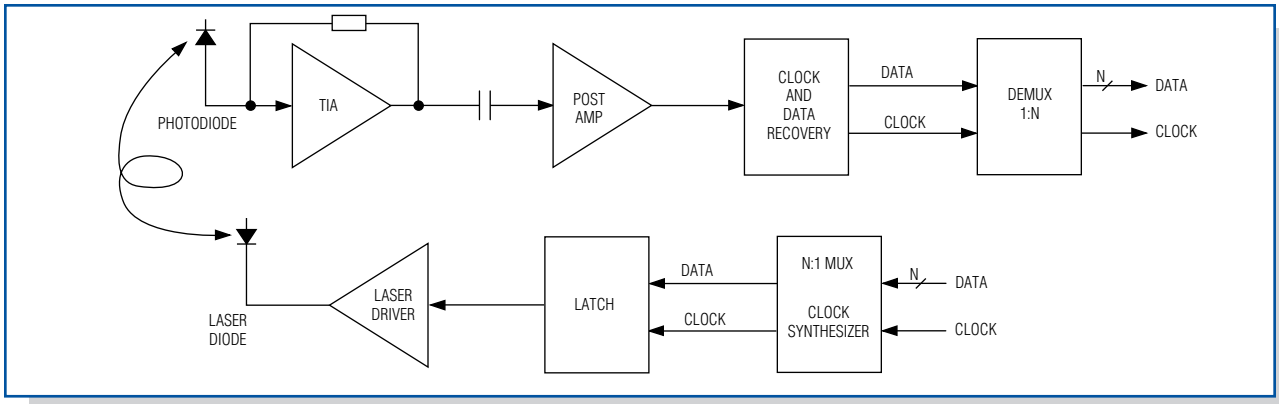


Figure 1. A typical receiver/transmitter unit for SONET/SDH fiber-transmission systems.

amplified by the TIA and (usually) converted to a differential signal as required by state-of-the-art receivers. The TIA should provide both high overload tolerance and high input sensitivity (i.e., a large dynamic range).

To provide the high input sensitivity necessary to receive optical signals weakened by transmitter aging or long transmission distance (or both), the TIA noise must be reduced to a minimum. On the other hand, a high overload tolerance is required to avoid bit errors due to distortion in the presence of strong optical signals. Further, the TIA's maximum achievable gain depends on the operating frequency. To ensure stable operation and the required bandwidth, gain can be optimized only within a narrow range. This limitation may cause the output voltage resulting from low-power optical signals to be insufficient for further processing. To amplify small TIA voltages in the 1mV to 2mV range, the TIA function must be followed by a postamplifier, which in most cases is a limiting amplifier (LA).

As the name implies, a limiting amplifier delivers a certain output-voltage swing whose maximum is independent of the input signal strength. Also included is a loss-of-power indicator (LOP) that warns when the incoming signal falls below a user-defined threshold. As a system-dependent parameter, this threshold must be adjusted externally. A comparator with hysteresis ensures chatter-free operation for the LOP flag when the signal is close to the threshold level.

A key component that follows the limiting amplifier in a receiver unit is the clock and data recovery (CDR) circuit. The CDR performs timing and amplitude-level decisions on the incoming signal, which leads to a time- and amplitude-regenerated data stream. First to be recovered from the received signal is the clock. Several possibilities can support this clock-recovery function (external SAW filter, external reference clock, etc.), but only the fully integrated approach can save both cost and effort.

The challenge for an integrated clock-recovery circuit is to meet the jitter specification recommended by the International Telecommunication Union-Telecom Standards Sector (ITU-T). Jitter refers to the effect in which individual bit transitions ("0" to "1" and vice-versa) are not exactly in phase. The effect becomes visual in an "eye diagram," in which several pseudo-random bit-pattern sequences are superimposed. An eye diagram illustrates the quality of a data stream in terms of the eye opening, measured using the "eye mask" **(Figure 2)**.

ITU-T recommendations specify limits on the tolerance, transfer, and generation of jitter. Signal quality at the LA output (as represented by the eye opening) is usually low, mostly as a consequence of nonideal components in the optical transmission system. Because the CDR must accept a certain amount of input data jitter to achieve normal error-free operation, all receiver units in line-termination and regenerator applications must comply with the ITU-T recommendations for jitter tolerance.

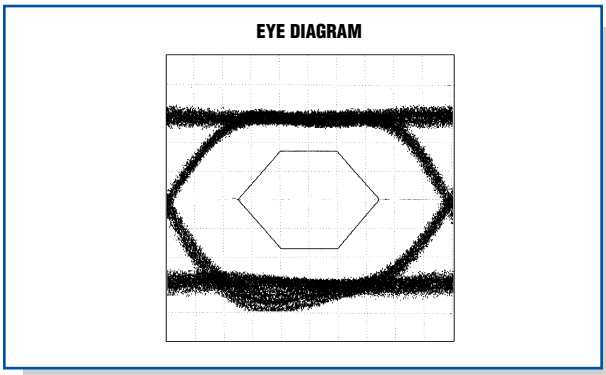


Figure 2. An "eye diagram" illustrates the signal quality of a data stream.

Jitter transfer refers to the portion of jitter allowed to transfer from input to output of the CDR, and jitter generation is that produced by the CDR itself. The ITU-T specs for these two parameters must be met for regenerators in a long-haul system, because at each stage the recovered clock enables transmission to the next regenerator, allowing jitter contributions to accumulate from regenerator to regenerator. Conversely, for line-termination receivers (which are in the majority of applications) the jitter transfer and jitter generation need not meet ITU-T recommendations. In those applications, the regenerated data is synchronized to the system clock.

Aside from jitter effects, noise and pulse distortion both reduce the phase margin in which received bits can be clocked for the purpose of sensing their logic level. The use of a phase-locked loop (PLL) is essential in synchronizing the clock with the data stream, to ensure alignment of the clock with the middle of a data word. To further optimize the bit error rate (BER) in the presence of asymmetrical rise and fall transitions of the received data signal, the system should include an option to adjust the phase relation between clock and data.

The CDR often includes a loss-of-lock (LOL) alarm, which monitors whether the PLL is locked to the received data stream. The CDR's serial stream of regenerated data and the recovered clock signal are usually fed to a deserializer, whose conversion ratio depends on the data's bit rate and the interface capability (speed) of the CMOS system components. The deserializer must also provide a CMOS-compatible interface. To support bit alignment of the serial data stream to the different deserializer outputs, the deserializer should include bit-synchronization capability.

Optical transmitter

The optical transmitter in a fiber optic system converts the electrical bit sequence delivered from the CMOS system components to an optical data stream. As shown in Figure 1, it contains a serializer with clock synthesizer (which depends on the system setup and transmission bit rate), a driver, and an optical source.

Two important wavelength ranges (windows 2 and 3) are in use for transmitting information over a fiber cable in telecommunication networks. Within an optical window, the signals benefit from a lower impact on quality (less dispersion) and less attenuation per unit of fiber length. The range between 1000nm and 1300nm, called the second optical window, is known for low dispersion—as low as 0dB. The range from 1500nm to 1800nm, known as the third optical window, offers the lowest attenuation per unit of fiber length **(Figure 3)**.

Several optical sources are available for today's optical transmission systems. Light-emitting diodes (LEDs), for example, are often used for low-cost, short-distance local area network (LAN) connections. Disadvantages, however, preclude use of the LED as a transmitter for telecommunications systems: its broad spectral bandwidth allows the coexistence of many optical modes, and it cannot operate at wavelengths of the second and third optical windows.

Unlike the LED, the optical-modulated laser transmitter (the electro-absorption and Mach-Zehnder types, for instance) is an optical source with high spectral purity that can operate in the third optical window. It is preferred, therefore, for ultra-long-distance or WDM transmission systems in which high performance is mandatory and cost is not a major consideration. For optical links in the majority of telecommunication trunk lines, various types of direct-modulated semiconductor laser diode offer an optimum cost/performance ratio for short, intermediate, and long-haul transmissions. Devices are available for operation in both the second and third optical windows.

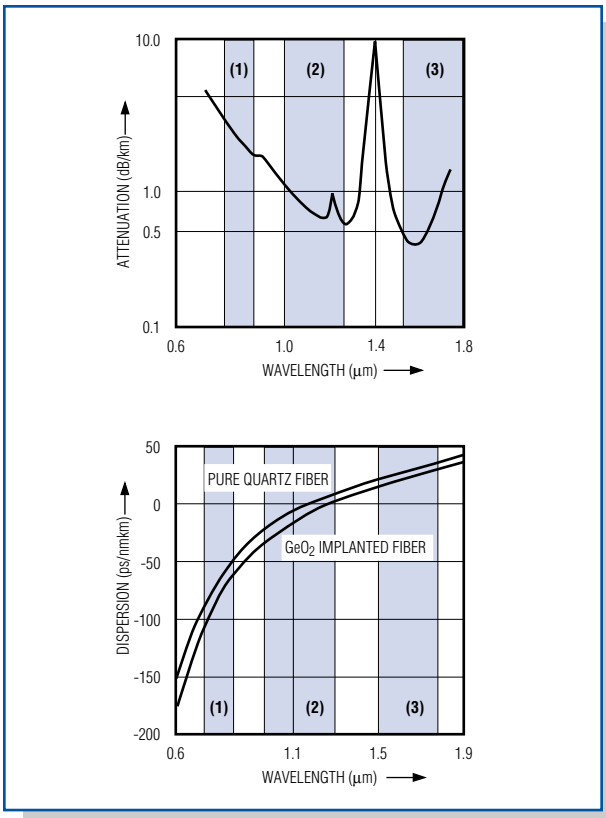


Figure 3. Variations of attenuation and dispersion vs. wavelength for the first, second, and third optical windows.

All semiconductor laser diodes used for direct modulation have in common the need for a DC-bias current to set the operating point and a modulation current for signal transmission. The values for DC-bias and modulation current depend on characteristics of the laser diode, which can differ from type to type and version to version. The drift of these characteristics with time and temperature should be evaluated carefully when designing a transmitter unit, especially with regard to the more cost-effective, uncooled types of semiconductor laser. The laser driver must therefore offer bias and modulation currents with sufficient range to support the development of optical transmitters with a wide choice of laser diodes.

To compensate for the drift of laser characteristics over time and temperature, the laser driver must maintain the initially adjusted DC operating point. The best way to realize this compensation is to introduce automatic power control (APC). To detect the actual laser power, a photodiode converts the laser light to a proportional current and feeds it to the laser driver, where the actual value is compared with a previous fixed value. Any difference causes the DC-bias current to increase or decrease as required to reach the initially defined laser power.

Often, the APC includes an alarm function that warns if the laser diode's optical power can no longer be sustained due to aging. Like the operating point, optical signal strength is affected by the drift of laser-diode characteristics over time and temperature. To maintain the optical "amplitude," it is necessary to compensate for a decreasing slope in these characteristics caused by time and temperature. The problem is solved either with additional external circuitry or with an integrated Automatic Modulation Control (AMC), which may employ the photodiode already present in the APC loop.

In addition to these fundamental functions, the system must be capable of stopping laser transmissions by disabling the driver without interrupting data reception at the input. By adding a flip-flop or latch (as part of the laser driver or the serializer), jitter performance can be improved by retiming this data stream before it reaches the laser driver's output stage.

Residing between the laser-diode driver and the lower-speed CMOS system components, the serializer converts parallel data to a serial stream for the laser driver. Like the receiver unit's deserializer, the serializer's conversion ratio depends on the transmission bit rate and the speed of the CMOS system interface. The retiming and serialization function requires a transmission clock, which must to be synthesized. This clock synthesizer can be integrated with the serializer, and usually incorporates a PLL. The challenge for the synthesizer is to ensure data transmission with the lowest possible jitter. As a result, the synthesizer plays a key role in the transmitter of an optical transmission system.

Complete chipset for STM 4 Rx/Tx units

All components of an optical transmission system for telecommunications must comply with the relevant ITU-T recommendations. Provided this basic requirement is met, the next most important criteria in designing an O/E unit are power dissipation, supply voltage, integration level, and margin of performance. The following section describes a complete chipset that allows designers to optimize the above criteria while developing competitive STM 4 receiver/transmitter units (**Figures 4** and **5**).

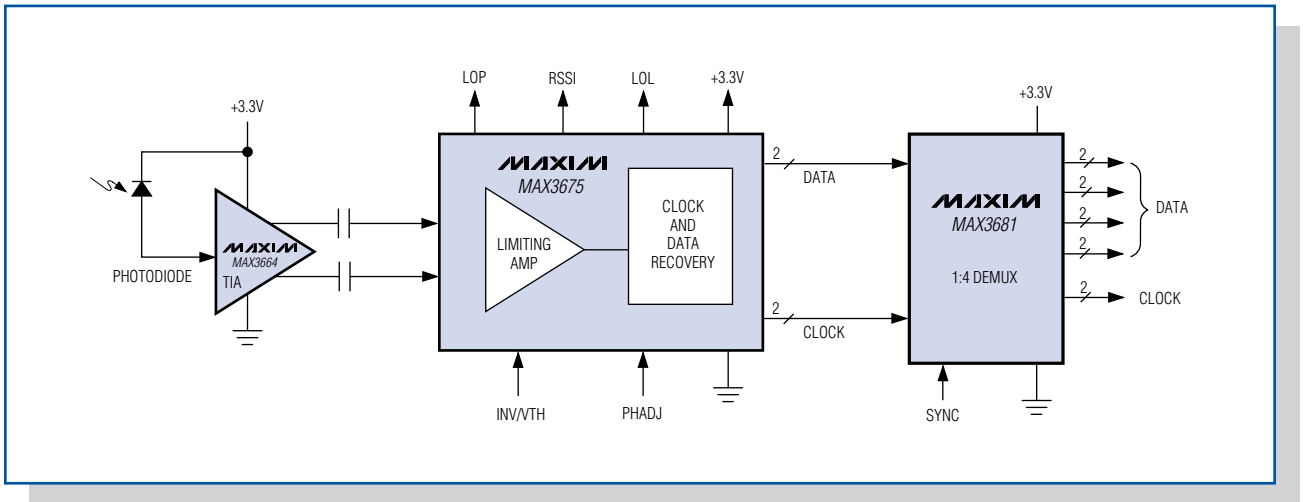


Figure 4. Three packages from Maxim form an STM 4 receiver.

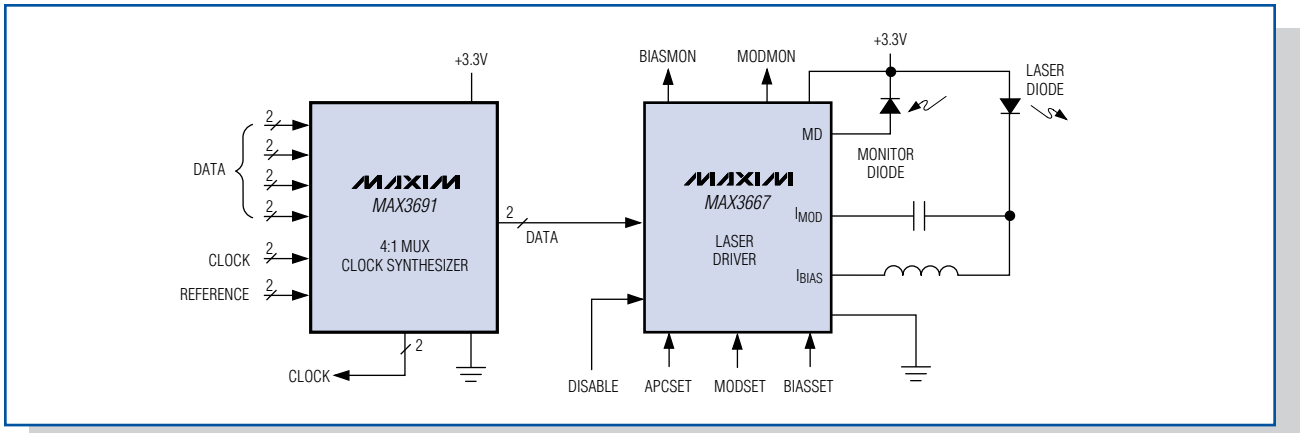


Figure 5. Two packages from Maxim form an STM 4 transmitter.

The chipset is based on Maxim's state-of-the-art, high-performance bipolar technologies: CB-2 and GST-2. CB-2 is a fast, complementary-bipolar process whose transit frequencies are 6.4GHz for pnp transistors and 8.7GHz for npn transistors. GST-2 is a very-high-speed, submicron bipolar process with a transit frequency of 27GHz for npn transistors.

The combination of modern high-performance manufacturing and extensive IC design experience has produced a highly integrated, flexible, and powerful STM 4 chipset consisting of five ICs including the serializer and deserializer. In serial-I/O modules the chipset consists of only three ICs, and they can be delivered in die form to accommodate "chip-on-board" mounting technology.

Power dissipation is an important consideration because system cooling requirements usually allow only a limited power budget in the O/E units. Maxim's STM 4 chipset makes extensive use of 27GHz, high-speed technology in reducing power dissipation. It can further reduce power dissipation by operating on +3.3V instead of today's more common +5V. Rather than require an additional source of +5V, the O/E unit can use the +3.3V available for CMOS system components. Or, to be flexible, it can share an existing +5V supply with the front-end ICs. In addition to these features, which pertain to the chipset as a whole, features specific to the individual components are described in the following sections.

Preamplifier (i.e., transimpedance amplifier)

The transimpedance amplifier (MAX3664) converts a single-ended current from the detector diode to a single-ended voltage, which is amplified and converted to a differential signal. Typical amplification is 6kΩ. This gain level can be increased by 6dB if the data outputs (back-terminated internally with 60Ω) are not externally terminated as well. For input currents beyond 100µAp-p, the high gain leads to a limited differential output-voltage swing of 900mVp-p. A DC-cancellation circuit helps to deliver differential output voltages with low pulse-width distortion over a wide range of input-current levels.

Low input-related noise is achieved by careful circuit design and by limiting the bandwidth to 590MHz at an input capacitance of 1.1pF. Assuming a simple PIN detector diode is used, the low noise enables a typical input sensitivity of -32dBm optical power. Power dissipation is less than 85mW at +3.3V. Small size and an optimal bondpad configuration make this component suitable for use in PIN-TIA modules, which combine a PIN diode and transimpedance amplifier in one package (a TO package, for instance).

Clock and Data Recovery (CDR)

The main functions of the clock and data recovery IC (MAX3675) are to recover the clock signal from the received data stream and to regenerate the data's timing and amplitude characteristics. Because the chip integrates an offset-compensated limiting amplifier as well, two standard products (MAX3664 and MAX3675) contain all the electronics necessary for an O/E receiver unit.

The MAX3675 offers a high-sensitivity differential analog input (3mVp-p) and a differential PECL digital input, providing flexibility that supports a wide range of receiver applications. The MAX3675's power dissipation depends on the input in use: 215mW with analog inputs, or 155mW with digital inputs. Total power consumption for a complete receiver based on the MAX3664 and MAX3675 is less than 300mW at +3.3V.

An LOP alarm function and input-power detector are integrated with the limiting amplifier. The LOP alarm

warns if the input signal falls below a user-defined threshold. The reference for this threshold is an internal bandgap circuit that is independent of the supply voltage. To ensure chatter-free operation for input signals near the threshold, the LOP's TTL-monitor output includes hysteresis. The power detector provides a receive signal-strength indicator (RSSI pin) whose output voltage is proportional to input power and is linear in decibels.

The PLL necessary for clock recovery is fully integrated and does not require an external reference clock. It consists of a phase/frequency detector, a loop-filter amplifier with external RC network, and a 622MHz voltage-controlled oscillator. The PLL provides an LOL signal (LOL pin) and a TTL-monitor output that flags when the PLL loses lock. To improve the system's bit error rate as described in the *Optical Receivers* section, users can adjust clock phase relative to the data signal by accessing the pins PHADJ+ and PHADJ-. Finally, a decision circuit supported by the recovered clock signal (from the PLL) regenerates timing and amplitude characteristics for the incoming data stream.

Deserializers (DEMUX)

To support the various CMOS system-interface circuits available today, Maxim offers the MAX3680 and MAX3681 deserializers. The MAX3680 converts a 622Mbps serial data stream to a 78Mbps stream of 8-bit words. Data and clock outputs are TTL compatible, and the power consumption is 165mW at +3.3V. The MAX3681 converts a 622Mbps serial data stream to a 155Mbps stream of 4-bit words. Its differential data and clock outputs support an LVDS interface for CMOS system components, and its power consumption is 265mW at +3.3V. Both parts offer serial differential-PECL inputs for data and clock, and a synchronization function (SYNC pin) that enables a bit realignment of the deserializer's data outputs.

Serializer (MUX)

The MAX3691 serializer converts four LVDS data streams at 155Mbps to a serial stream at 622Mbps. The necessary transmission clock is synthesized using a fully integrated PLL comprising a voltage-controlled oscillator, a loop-filter amplifier, and a phase/frequency detector that requires only an external reference clock. All the data- and clock-input buffers are LVDS-compatible, and the serial data output delivers differential-PECL signals. Power dissipation is 215mW at +3.3V.

Laser Driver (LD)

The main task of the laser driver (MAX3667) is to deliver the bias (I_{BIAS}) and modulation current (I_{MOD}) for a direct-modulated laser diode. For flexibility, the differential inputs accept PECL data streams and also differential voltage swings as small as 320mVp-p, with DC levels in the range 1V to (V_{CC} - 0.75V). Connecting an external resistor between BIASSET and ground lets you adjust the bias current between 5mA and 90mA, and a resistor between MODSET and ground lets you adjust the modulation current between 5mA and 60mA.

An integrated, temperature-stabilized reference voltage ensures stable bias and modulation currents. To avoid laser damage, a protection circuit disables the MAX3667 when any of the pins BIASSET, MODSET, or APCSET are short-circuited to ground. To avoid excessive current that could alter the laser's performance, an internal circuit also limits the sum of output currents I_{MOD} and I_{BIAS} to approximately 150mA. As described in the *Optical Transmitter* section, an integrated APC circuit, supported by an external detector diode, maintains the initial user-defined average laser power constant over time and temperature.

The detector diode's average current value is established by applying an external resistor between the APCSET and GND pins. Two monitor outputs (BIASMON and MODMON) deliver output currents directly proportional to the bias and modulation currents. The bias, modulation, and APCSET currents can be disabled via the DISABLE pin, but all other functions including the reference voltage remain active to allow a fast and predictable wake-up. In addition, an integrated slow-start function provides a 50ns minimum turn-on time that reduces laser stress. In contrast to other laser drivers available in today's market, the MAX3667 can operate from a single +3.3V supply.

As an alternative to the 622Mbps MAX3667, the MAX3766 laser driver can be used for STM 4 transmitter units supporting data rates from 155Mbps to 1.25Gbps. Designed to operate on a single +5V supply, the MAX3766 incorporates all attributes mentioned for the MAX3667 plus the larger bandwidth (to 1.25Gbps). Other features include extensive laser-safety provisions and the option to add a single external resistor that maintains "optical amplitude" by compensating for the effect of temperature on the slope of the characteristic laser curve. The resistor's value depends on the laser diode's temperature characteristic.

Driving a laser diode at 622Mbps from a single +3.3V power supply

As fiber communication systems continue to move into the home, equipment manufacturers are being driven more than ever to reduce power consumption. Reducing the power-supply requirements into a single +3.3V supply is one obvious way to significantly improve the overall power dissipation of any system. But finding a laser transmitter that operates properly in a single +3.3V environment, while still meeting the stringent jitter and optical transmission requirements typical of SDH/SONET telecommunications, is a difficult challenge.

High current requirements, fast switching capability, and laser lead inductances all work against achieving the +3.3V goal. Maxim's new MAX3667 laser driver, part of Maxim's complete +3.3V, 622Mbps fiber communication solutions **(Figure 1)**, overcomes these challenges and provides a unique solution.

The operating temperature range for telecommunications covers -40°C to +85°C. Over this range, the required threshold current for laser diodes will vary significantly. It is not uncommon for the laser's threshold level to move by more than 40mA between -40°C and +85°C **(Figure 2)**.

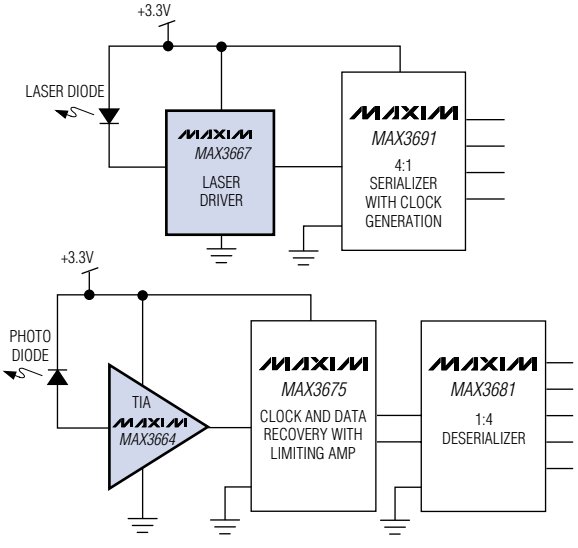


Figure 1. Maxim's +3.3V, 622Mbps Chipset

Typical long-wavelength, Fabry-Perot-style laser diodes require forward bias voltages on the order of 1.2V. This forward bias requirement is a function of the energy gap associated with the laser diode and can be greater than 1.6V. The forward voltage drop, together with a +3.3V ±5% supply, means as little as 1.5V could be all that remains for the laser driver output stage. Within this tight constraint, the laser driver must provide both a bias current (I_{BIAS}) to set the laser diode above threshold and a modulation current (I_{MOD}) to transmit the data. Bias current requirements as high as 60mA are typical and, depending on the distance requirements, modulation currents could exceed 60mA. At the same time, the output signal must be fast enough to meet the stringent jitter generation requirements as well as the transmission eye diagram of SDH/SONET.

Figure 3 shows a laser diode and the inductance associated with the package. In this configuration, a total current of $I_{BIAS} + I_{MOD}$ must flow through both the laser diode and the inductance.

The total voltage drop at the output of the laser driver is 1.6V + $L\Delta i/\Delta t$. For 622Mbps applications, optical edge speeds of less than 600ps (electrical) are typical, resulting in an additional voltage transient across the inductor as high as:

$$V_L = 5nH\ (60mA) / 600ps = 500mV$$

This results in an output voltage requirement for the laser driver of +3.1V - 1.6V - 0.5V = 1.0V.

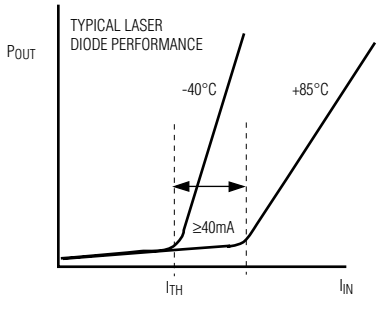


Figure 2. Laser diode threshold vs. temperature

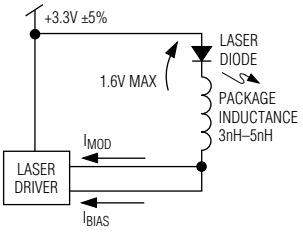


Figure 3. DC-coupled laser

The traditional bias current output stage is a simple current source capable of operating within such a tight operating voltage. On the other hand, the modulation current output stage is typically a switching differential pair, requiring more than two V_{BE} (base emitter voltage) of headroom and making it impossible to operate with such low output voltage requirements. The MAX3667 incorporates a high-speed current source architecture capable of operating within the reduced headroom **(Figure 4)**.

By isolating the output stage from the DC voltage drop associated with the laser diode, the I_{MOD} output can operate closer to the supply voltage and thus further relax the headroom constraints **(Figure 5)**.

Maxim's MAX3667 laser driver allows AC-coupling of the I_{MOD} output by providing an integrated pull-up resistor for self-biasing and enough current drive capability to overcome the additional loading of such a technique. The total modulation current available at the output of the MAX3667 actually exceeds 100mAp-p. The internal pull-up resistor of 31Ω, as well as the damping and matching resistors expected when interfacing to laser diodes at high speeds, results in a reduction of the total modulation current made available at the laser diode. For typical resistor values, this current is divided down to approximately 60mAp-p.

There are trade-offs to AC-coupling the modulation current. By introducing a capacitor into the signal path, a low-frequency cutoff has been added to the system. SDH/SONET signals consist of non-return-to-zero data streams. Typical expectations for these systems are that they will maintain a 10^{-10} bit error

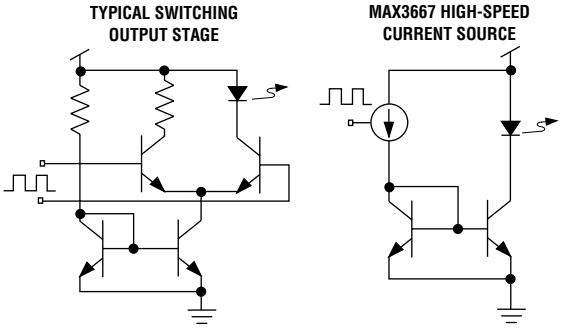


Figure 4. Different laser driver output stages

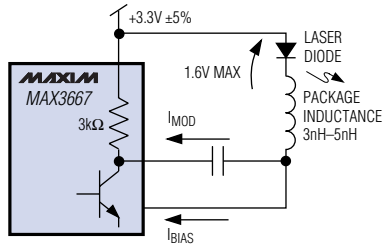


Figure 5. AC-coupled modulation current

rate with up to 72 consecutive 1s or 0s. This low-frequency requirement, together with the time constant associated with the DC-blocking capacitor, can greatly affect the pattern-dependent jitter (PDJ) at the output of the laser diode. It is important that this time constant result in minimum output droop associated with the long consecutive bit streams. Obviously, this problem can easily be solved by using a large capacitor for the coupling capacitor, but this works against the typical design goal of reducing the size of the optical transmitter. By using an AC-coupling capacitor no bigger than 1µF, the MAX3667 can achieve low output droop and low PDJ for consecutive bit streams greater than 100 bits.

The MAX3667 can operate a laser diode from a single +3.3V supply. In addition to providing enough drive capability, it contains a fully integrated APC loop for maintaining the bias current over temperature. The MAX3667 easily meets ITU and Bellcore jitter generation specifications for 622Mbps transmitters, without increasing cost or layout complexity.

Design challenges for fiber optic LAN transceivers

Designing fiber optic transmitters and receivers for Local Area Network (LAN) applications presents unique design challenges that are different from those found in longer-distance regulated telecommunications applications. This article examines the issues involved in designing transmitters and receivers for LAN applications.

Transmitters

The transmitter in a LAN/data communications transceiver generally consists of a driver and an optical emitting device. This device can be an LED, laser, or VCSEL (Vertical Cavity Surface Emitting Laser). The driver must convert digital data into current pulses that cause the emitter to generate light.

Interfacing with an LED, laser, or VCSEL is not straightforward. These devices typically have a forward voltage between 1.3V and 2.0V. This becomes critical when V_{CC} drops to 3.0V. The optical devices usually require a current drive capability between 10mA and 60mA to produce the desired optical output power. Also, the voltage swing due to packaging inductance of the optical device must be considered.

TRANSMITTER REQUIREMENT	DRIVER CONSIDERATION(S)
CW Output Power Requirement	DC output (bias) current amplitude, accuracy, Automatic Power Control feature
Extinction Ratio	Modulation output current amplitude and accuracy, tempco of laser modulation current
Eye Diagram	Controlled output current (ringing, overshoot well behaved, edge speed within proper range)
Eye Safety	Single-point fault protection
Jitter Generation	Low jitter, low noise

A typical application is an emitting device for Gigabit Ethernet packaged in a TO-46 header, with 8nH of lead inductance. The required rise time for Gigabit Ethernet is approximately 300ps. Each rising edge of data requires 8nH (30mA/300ps) 800mV of voltage swing if $V_L = L\Delta i/\Delta t$ and the required laser current is 30mA. The same voltage with opposite polarity is required on the falling edge of data, creating an AC voltage requirement of 1.6V. The total voltage headroom requirement is 3.0V or more when combined with the DC forward voltage of the laser diode. This is one of the challenges to address when designing a 3V laser driver.

The standards for fiber optic data communications typically require the transmitter's output power to remain within a narrow range. Maintaining the power in this range is difficult, however, because the optical efficiency of the emitting devices varies with age and temperature. Maxim's laser drivers include a feedback control loop for Automatic Power Control (APC), so average power is maintained.

Another transmitter requirement is the extinction ratio, which is the ratio of power level between a one and a zero. This specification ensures that there is sufficient signal present in the optical signal. Again, this specification is a design challenge because the optical emitter efficiency changes substantially with temperature. A typical 1300nm laser requires 10mA of drive current at +25°C and 30mA at +50°C. Maxim laser drivers solve this problem using a variety of methods. The MAX3766, MAX3286, and MAX3296 provide a temperature compensation adjustment that increases the modulator output current with temperature. This feature can be adjusted to compensate for changes in the laser efficiency.

Eye safety is a common transmitter requirement, especially for short wavelength (780nm to 850nm), multimode fiber applications. This wavelength causes damage to the human eye if applied with sufficient power. Transmitter designers employ the APC scheme previously discussed to prevent this problem. But the feedback loop can be broken by faults in the circuit, which means the APC circuit could cause the output power to increase beyond the

safe level if a critical point in the circuit was accidentally shorted to V_{CC} or GND. The industry standard regarding eye safety calls for tolerance to a single-point fault. Maxim's MAX3766, MAX3286†, and MAX3296† are single-point fault tolerant. Any point in the circuit can be shorted to V_{CC} or GND without causing an unsafe transmitter power output.

Operation of the APC loop during startup is also an issue. Some APC circuits may not work correctly at turn-on, or they may produce very high transmitter power during turn-on. This problem can cause the driver output current to exceed the laser's absolute maximum ratings, possibly damaging the laser. Maxim laser drivers use a proprietary "smooth start-up" circuit to prevent laser damage.

Receivers

A typical receiver comprises a photodetector (photodiode), transimpedance amplifier (TIA), and limiting amplifier (quantizer). The photodiode converts light pulses to current pulses that are amplified by the TIA and then output as voltage pulses. The limiting amplifier provides the binary decision. Typical input to a 622Mbps optical LAN receiver may be as small as -28dBm with an extinction ratio of 10, which provides a 3µAp-p signal at the photodetector.

RECEIVER REQUIREMENT	CONSIDERATION(S)
Sensitivity (smallest input)	Input-referred noise, gain, bandwidth
Overload (largest input)	Maximum current input to transimpedance amplifier
Jitter	Pulse width distortion, data-dependent jitter, random jitter from noise
Signal Detect	Gain, range of signal detect, type of signal detect, hysteresis of signal detect

The total gain between the TIA and the limiting amplifier must be at least 1.6V/3µA = 530 (114dB) to obtain digital PECL receiver output. This gain is spread between the TIA and limiting amplifier to prevent oscillations.

The TIA's input-referred noise generally determines the sensitivity of the receiver. This noise must be kept as small as possible to obtain good sensitivity and maximum link distance. The TIA typically tolerates signals as large as 1mAp-p. These low-noise, high dynamic range restraints make TIA design difficult.

The limiting amplifier has up to 50dB to 70dB gain and performs the quantizing, or decision making, function. A signal-detect circuit is usually provided inside the limiting amplifier. The signal-detect circuit is most effective if it detects the AC portion of the signal, not the DC component. The signal-detect output is used by the digital circuitry further downstream to determine if the input signal contains valid data, or is just noise. The limiting amplifier output is typically PECL-compatible. Driving inductive cables and connectors at high speed becomes an important issue for data rates above 300Mbps. The MAX3264† and MAX3265† use a current-mode output that is virtually insensitive to load inductance.

†*MAX3264/MAX3265/MAX3286/MAX3296 are future products.*

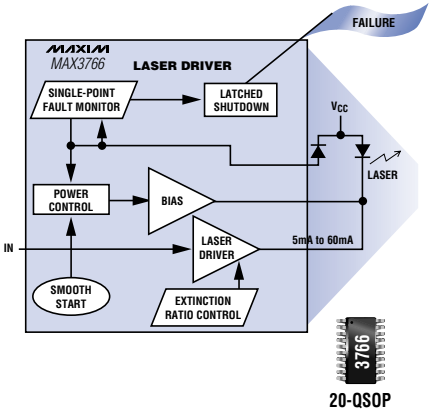
NEW PRODUCTS

622Mbps LAN/ATM laser driver has tempco adjustment, safety features, and modulation current

The MAX3766 laser driver is specially designed for fiber optic LAN transmitters and optimized for operation at 622Mbps. It includes a laser modulator, automatic power control (APC) circuitry, and a fail indicator with latched shutdown.

An external resistor programs the laser's modulation current (the maximum at 622Mbps is 60mA). Another resistor programs the laser's bias current between 0.5mA and 80mA. At lower modulation currents, the MAX3766 can operate at data rates to 1.25Gbps. The temperature coefficient of modulation can also be programmed to keep the transmitted extinction ratio nearly constant over a wide temperature range. APC circuitry, using feedback from the laser's monitor photodiode, adjusts the laser's bias current to produce a constant output power regardless of the laser's temperature or age.

To ensure that the transmitter output does not reach hazardous levels, the MAX3766 provides extensive laser-safety measures, including a failure indicator with latched shutdown and a smooth-startup bias generator. The MAX3766 is available in a 20-pin QSOP package.



3.3V, 622Mbps, SDH/SONET 8:1 serializer includes clock synthesis and TTL inputs

The MAX3690 serializer operates from a +3.3V supply, consumes 200mW, and converts 8-bit-wide, 77MHz parallel data to 622Mbps serial data in SDH/SONET systems. Other applications include add/drop multiplexers and digital cross connects.

The MAX3690 accepts TTL clock and data inputs, and delivers a 3.3V PECL serial-data output. A fully integrated phase-locked loop (PLL) synthesizes an internal 622Mbps serial clock from a low-speed crystal reference clock of 77.76MHz, 38.88MHz, or 51.84MHz. A TTL loss-of-lock output indicates whether the PLL is operating correctly.

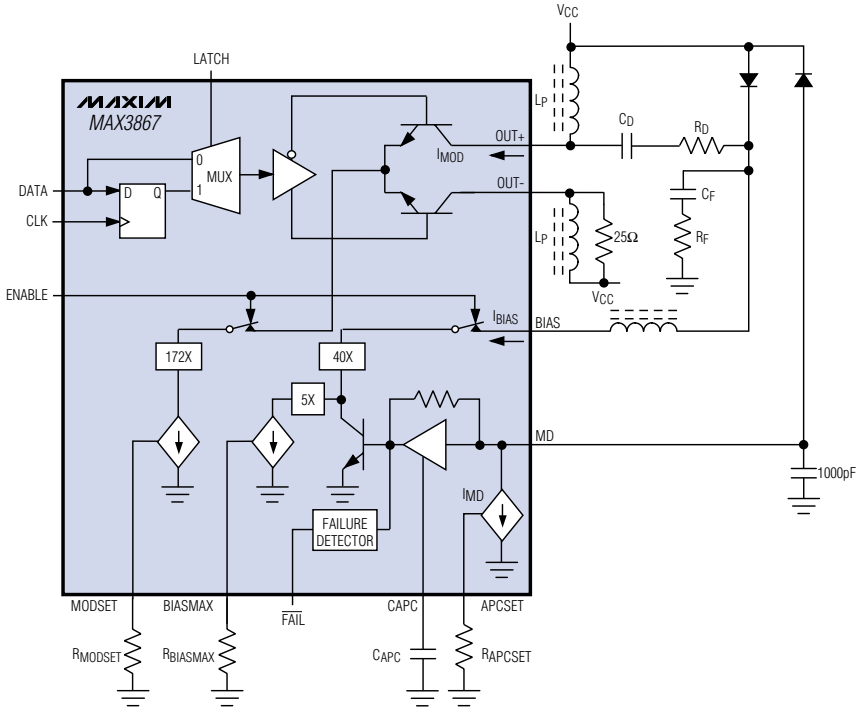
The MAX3690 is available in a 32-pin TQFP package.

3.3V, 2.5Gbps, SDH/SONET laser driver has automatic power control

The MAX3867 laser driver operates on +3.3V or +5V supplies and draws less than 65mA of supply current at +3.3V. It accepts differential-PECL data and clock inputs to 2.5Gbps, and provides bias and modulation currents for the laser. The synchronizing input latch can be bypassed if a clock signal is not available.

Automatic power control (APC) feedback maintains a constant average optical power over temperature and lifetime. The wide ranges of modulation current (5mA to 60mA) and bias current (1mA to 100mA) are easy to program, making the MAX3867 an excellent choice for various SDH/SONET applications. It complies with ANSI, ITU, and Bellcore SDH/SONET specifications.

The MAX3867 also provides an enable control, a programmable slow-start circuit for setting the laser turn-on delay, and a failure-monitor output that indicates when the APC loop is unable to maintain the average optical power. It is available in a small 48-pin TQFP.



NEW PRODUCTS

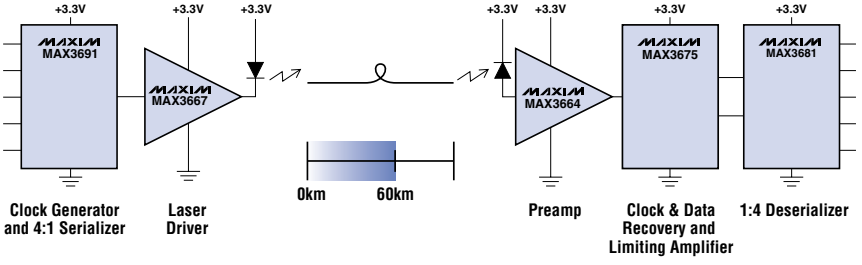
3.3V, 622Mbps SDH/SONET laser driver has APC

The MAX3667 is a complete +3.3V (or +5V) laser-diode driver. Designed for SDH/SONET applications operating to 622Mbps, it includes automatic power control (APC) to compensate for changes in the laser efficiency due to temperature effects and aging.

The MAX3667 accepts differential-PECL inputs and provides single-ended bias and modulation currents for the laser diode. An internal, temperature-stabilized reference voltage simplifies the external programming of these currents, providing a 5mAp-p to 60mAp-p range for the modulation current and a 5mA to 90mA range for the bias current.

To aid external circuitry in supervising the performance of the laser-driver system, two internal monitors provide high-speed analog currents that are directly proportional to the bias and modulation currents. Other features include enable/disable control and a slow-start capability with 50ns minimum turn-on time. The MAX3667 is available in a 32-pin TQFP package specified for the extended-industrial temperature range (-40°C to +85°C).

Complete 3.3V Transmitter/Receiver Chipset Includes Clock Generator and Serializer



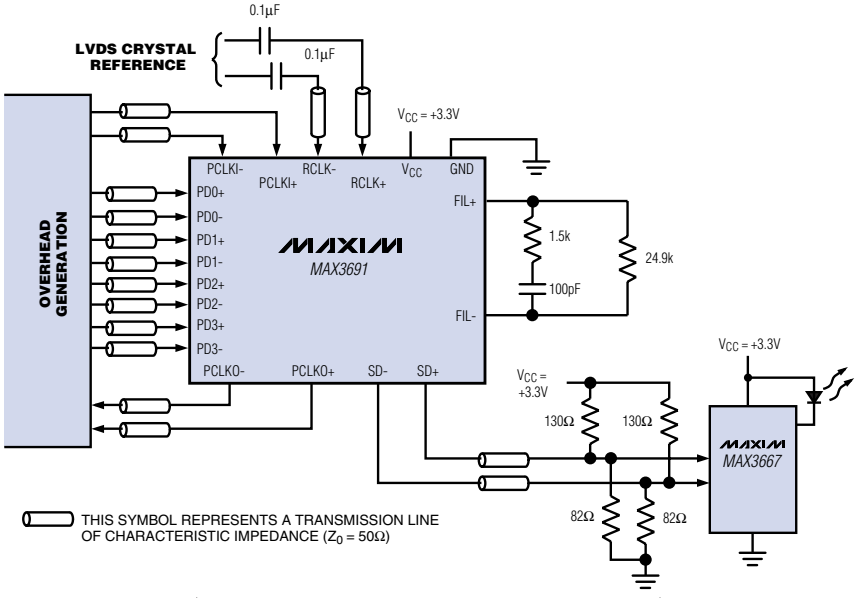
622Mbps, 4:1 SDH/SONET serializer features LVDS inputs, PLL clock synthesizer

The MAX3691 4:1 serializer is designed to convert 155Mbps parallel data to 622Mbps serial data in 622Mbps SDH/SONET applications. Operating from a +3.3V supply, it provides a high-speed digital interface by accepting low-voltage differential-signal (LVDS) clock and data inputs, and delivering a 3.3V differential-PECL serial-data output.

The MAX3691 includes a fully integrated phase-locked loop (PLL) consisting of a phase/frequency detector, loop filter/amplifier, and voltage-controlled oscillator, which synthesizes an internal 622Mbps serial clock from a low-speed crystal-reference clock. By locking onto an external reference of 155.52MHz, the PLL generates an internal 622Mbps for clocking the output shift register. A TTL loss-of-lock output indicates whether the PLL is operating properly.

Along with the MAX3667 laser driver, the MAX3691 is part of a 2-chip complete solution for 622Mbps SDH/SONET applications. Their +3.3V power supplies, PECL input (MAX3667), and PECL output (MAX3691) simplify the design of 622Msps transmission systems.

The MAX3691 is available in a 32-pin TQFP package specified for the extended-industrial temperature range (-40°C to +85°C).



NEW PRODUCTS

622Mbps low-noise transimpedance preamplifier serves optical receivers in LAN and WAN systems

The MAX3760 is a transimpedance preamplifier for 622Mbps ATM applications. It converts small photodiode currents to measurable differential voltages, and includes a DC-cancellation circuit that reduces pulse width distortion by providing true differential output swings over a wide range of current levels. It operates from a single +5V supply and has a typical power consumption of 100mW.

The MAX3760 has a 6.5kΩ transimpedance gain, 560MHz bandwidth, and handles input overloads to 1mA. With an operating temperature range of -40°C to +85°C, its low input-referred noise (73nA) allows a typical input sensitivity of -31.5dBm for 1300nm receivers. Typical optical-input overloads (-3dBm) give an overall dynamic range of 28.5dB.

This preamplifier is internally compensated and requires few external components. In die form its space-saving filter connection provides positive bias for the photodiode through a 1kΩ resistor to V_{CC}. These features allow the MAX3760 and photodiode to be easily assembled in a TO-style header. The MAX3760 is designed for use with the MAX3761 or MAX3762 limiting amplifier. When combined with a photodiode, the resulting chipset forms a complete 5V, 622Mbps receiver. The MAX3760 is available as die or in an 8-pin SO package.

3.3V, 2.488Gbps, SDH/SONET 1:16 deserializer has LVDS outputs

The MAX3885 deserializer converts 2.488Gbps serial data to 16-bit-wide, 155Mbps parallel data in SDH/SONET systems. Other applications include add/drop multiplexers and digital cross connects.

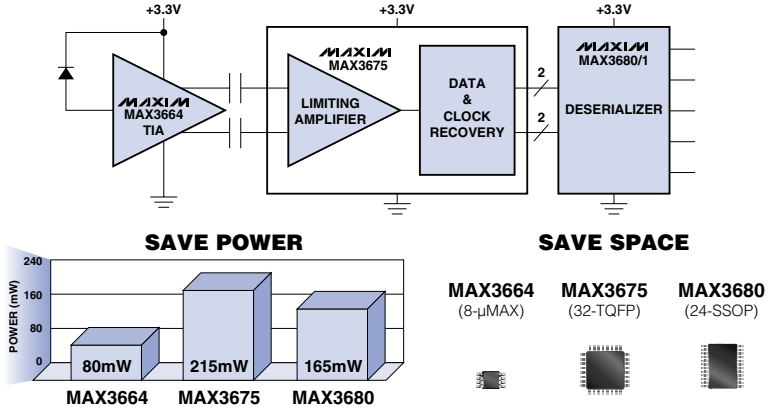
As an interface to high-speed digital circuitry, the MAX3885 accepts data and clock inputs in a PECL serial format, and delivers clock and data outputs in a low-voltage differential-signal (LVDS) format. It operates from a single +3.3V supply and draws 630mW. In addition, its LVDS synchronization input enables data realignment and reframing, and its self-biasing PECL inputs simplify AC coupling. The MAX3885 comes in a 64-pin TQFP package.

622Mbps, SDH/SONET 1:8 deserializer has TTL outputs and draws 265mW

The MAX3680 deserializer is a bipolar IC that includes input and output buffers, an 8-bit shift register, and an 8-bit parallel output register. Designed to convert 622Mbps serial data to 8-bit-wide, 77Mbps parallel data, the MAX3680 is suitable for use in SDH/SONET transmission systems, ATM/SONET access nodes, add/drop multiplexers, and digital cross connects.

The MAX3680 operates from a single +3.3V supply and consumes 265mW (typ) in normal operation. It accepts PECL-compatible serial clock and data inputs and delivers TTL-compatible outputs. It also includes a TTL-synchronization input that enables data realignment and framing as part of the interface to external, high-speed digital circuitry.

The MAX3680 comes in a 28-pin SSOP package specified for the extended-industrial temperature range (-40°C to +85°C).



2.5Gbps, low-power clock-recovery and data-retiming IC operates on 3.3V

The MAX3875 is a compact, low-power clock-recovery and data-retiming IC for 2.488Gbps SDH/SONET applications. Its fully integrated phase-locked loop recovers a synchronous clock signal from the serial NRZ data input, which is then retimed by the recovered clock. Differential PECL-compatible outputs are provided for both clock and data signals, and the chip provides an additional 2.488Gbps serial input for system-loopback diagnostic testing. It also provides a TTL-compatible loss-of-lock (LOL) monitor.

The MAX3875 is designed for both section-regenerator and terminal-receiver applications in OC-48/STM-16 transmission systems. Its jitter performance exceeds all SDH/SONET specifications. It operates from a single supply voltage of +3.3V to +5V. At +3.3V, it consumes only 400mW over the extended-industrial temperature range (-40°C to +85°C). The MAX3875 is available in a 32-pin TQFP package.